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DATA SHEET

SAA7182; SAA7183
Digital Video Encoder (EURO-DENC)

Preliminary specification
Supersedes data of 1995 Sep 19
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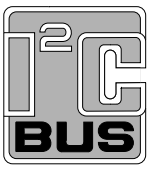
Philips Semiconductors

PHILIPS

Digital Video Encoder (EURO-DENC) SAA7182; SAA7183

FEATURES



- CMOS 5 V device
- Digital PAL/NTSC/SECAM encoder
- System pixel frequency 13.5 MHz
- Accepts MPEG decoded data on 8-bit wide input port. Input data format Cb, Y, Cr etc. or Y and Cb, Cr on 16 lines (*"CCIR 656"*)
- Three DACs for CVBS, Y and C operating at 27 MHz with 10-bit resolution
- Three DACs for RGB operating at 27 MHz with 9-bit resolution, RGB sync on CVBS and Y
- CVBS, Y, C and RGB output simultaneously
- Closed captioning and teletext encoding including sequencer and filter
- On-chip YUV to RGB matrix
- Fast I^{2}C-bus control port (400 kHz)
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- Internal Colour Bar Generator (CBG)
- Overlay with Look-Up Tables (LUTs) 8×3 bytes
- Macrovision Pay-per-View protection system as option, also used for RGB output

  This applies to SAA7183 only. The device is protected by USA patent numbers 461603, 4577216 and 4819098 and other intellectual property rights.

  Use of the Macrovision anti-copy process in the device is licensed for non-commercial home use only. Reverse engineering or disassembly is prohibited. Please contact your nearest Philips Semiconductor sales office for more information
- Controlled rise/fall times of output syncs and blanking
- Down-mode of DACs
- PLCC84 package.

GENERAL DESCRIPTION

The SAA7182; SAA7183 encodes digital YUV video data to an NTSC, PAL, SECAM CVBS or S-Video signal and also RGB.

The circuit accepts CCIR compatible YUV data with 720 active pixels per line in 4 : 2 : 2 multiplexed formats, for example MPEG decoded data. It includes a sync/clock generator and on-chip Digital-to-Analog Converters (DACs).

The circuit is compatible to the DIG-TV2 chip family.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	4.75	5.0	5.25	V
V_{DDD}	digital supply voltage	4.75	5.0	5.25	V
I_{DDA}	analog supply current	–	90	110	mA
I_{DDD}	digital supply current	–	220	250	mA
V_i	input signal voltage levels	TTL compatible			
$V_{o(p-p)}$	analog output signal voltages Y, C, CVBS and RGB without load (peak-to-peak value)	–	2	–	V
R_L	load resistance	80	–	–	Ω
ILE	LF integral linearity error	–	–	±2	LSB
DLE	LF differential linearity error	–	–	±1	LSB
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7182WP	PLCC84	plastic leaded chip carrier; 84 leads	SOT189-2
SAA7183WP	PLCC84	plastic leaded chip carrier; 84 leads	SOT189-2

BLOCK DIAGRAM

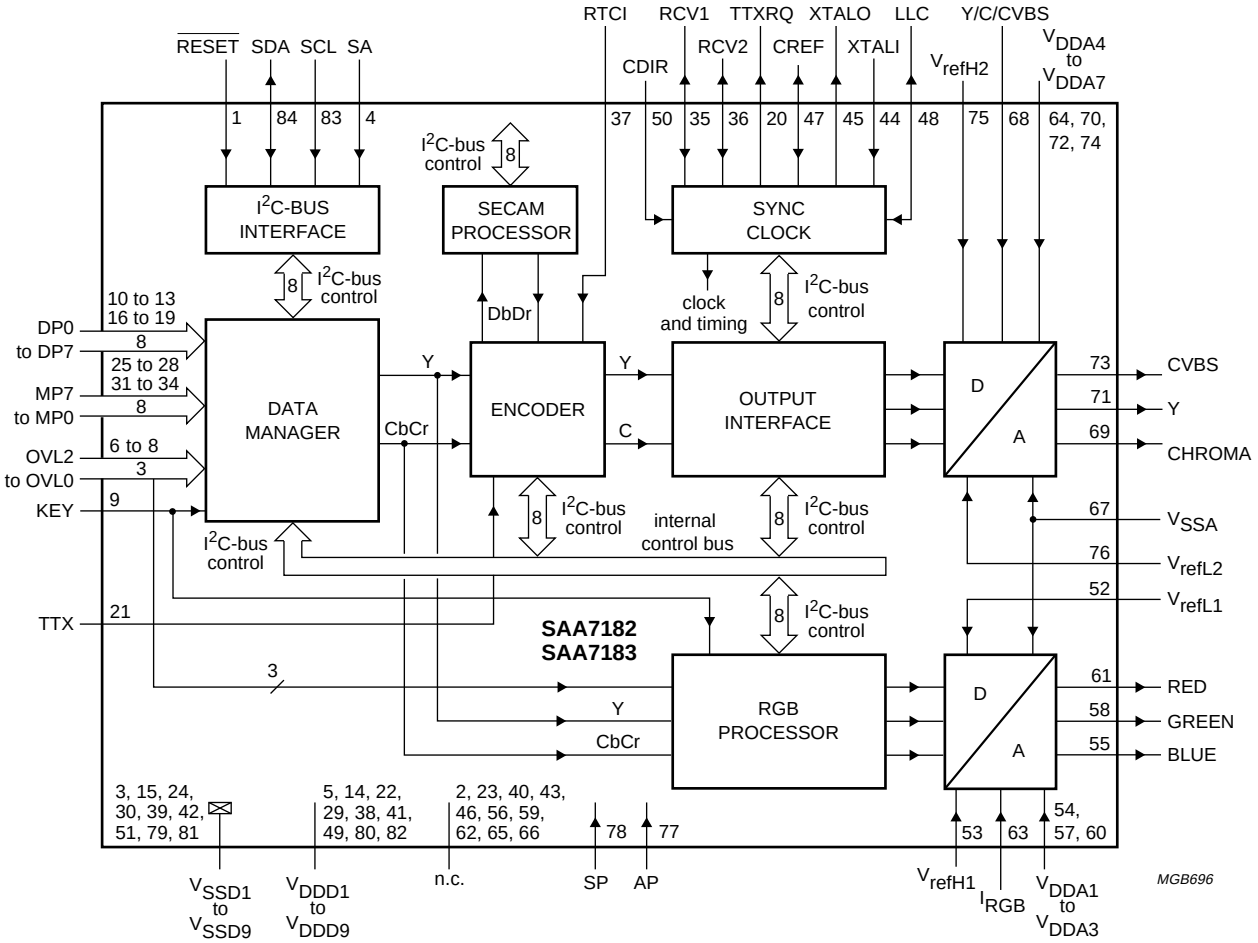


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{\text{RESET}}$	1	Reset input, active LOW. After reset is applied, all digital I/Os are in input mode. The I^2C-bus receiver waits for the START condition.
n.c.	2	not connected
V_{SSD1}	3	digital ground 1
SA	4	The I^2C-bus slave address select pin. LOW: slave address = 88H, HIGH = 8CH.
V_{DDD1}	5	digital supply voltage 1
OVL2	6	3-bit overlay data input. This is the index for the internal look-up table.
OVL1	7	
OVL0	8	
KEY	9	Key input for OVL. When HIGH it selects OVL input.
DP0	10	Lower 4 bits of the data port. Input for multiplexed Cb, Cr data if 16 line input mode is used.
DP1	11	
DP2	12	
DP3	13	
V_{DDD2}	14	digital supply voltage 2
V_{SSD2}	15	digital ground 2
DP4	16	Upper 4 bits of the data port. Input for multiplexed Cb, Cr data if 16 line input mode is used.
DP5	17	
DP6	18	
DP7	19	
TTXRQ	20	Teletext request output, indicating when the bitstream is valid.
TTX	21	Teletext bitstream input.
V_{DDD3}	22	digital supply voltage 3
n.c.	23	not connected
V_{SSD3}	24	digital ground 3
MP7	25	Upper 4 bits of MPEG port. It is an input for *"CCIR 656"* style multiplexed Cb, Y, Cr data, or input for Y data only, if 16 line input mode is used.
MP6	26	
MP5	27	
MP4	28	
V_{DDD4}	29	digital supply voltage 4
V_{SSD4}	30	digital ground 4
MP3	31	Lower 4 bits of MPEG port. It is an input for *"CCIR 656"* style multiplexed Cb, Y, Cr data, or input for Y data only, if 16 line input mode is used.
MP2	32	
MP1	33	
MP0	34	
RCV1	35	Raster Control 1 for video port. This pin receives/provides a VS/FS/FSEQ signal.
RCV2	36	Raster Control 2 for video port. This pin provides an HS pulse of programmable length or receives an HS pulse.
RTCI	37	Real Time Control Input. If the LLC clock is provided by an *SAA7111* or *SAA7151B*, RTCI should be connected to the RTCO pin of the respective decoder to improve the signal quality.

SYMBOL	PIN	DESCRIPTION
V_{DDD5}	38	digital supply voltage 5
V_{SSD5}	39	digital ground 5
n.c.	40	not connected
V_{DDD6}	41	digital supply voltage 6
V_{SSD6}	42	digital ground 6
n.c.	43	not connected
XTALI	44	Crystal oscillator input (from crystal). If the oscillator is not used, this pin should be connected to ground.
XTALO	45	Crystal oscillator output (to crystal).
n.c.	46	not connected
CREF	47	Clock Reference signal. This is the clock qualifier for DIG-TV2 compatible signals.
LLC	48	Line-Locked Clock. This is the 27 MHz master clock for the encoder. The I/O direction is set by the CDIR pin.
V_{DDD7}	49	digital supply voltage 7
CDIR	50	Clock direction. If the CDIR input is HIGH, the circuit receives a clock and optional CREF signal, otherwise if CDIR is LOW CREF and LLC are generated by the internal crystal oscillator.
V_{SSD7}	51	digital ground 7
V_{refL1}	52	Lower reference voltage 1 input for the RGB DACs, connect to V_{SSA}.
V_{refH1}	53	Upper reference voltage 1 input for the RGB DACs, connect via 100 nF capacitor to $V_{SSA.}$
V_{DDA1}	54	Analog supply voltage 1 for the RGB DACs.
BLUE	55	Analog output of the BLUE component.
n.c.	56	not connected
V_{DDA2}	57	Analog supply voltage 2 for the RGB DACs.
GREEN	58	Analog output of the GREEN component.
n.c.	59	not connected
V_{DDA3}	60	Analog supply voltage 3 for the RGB DACs.
RED	61	Analog output of the RED component.
n.c.	62	not connected
I_{RGB}	63	Current input for RGB amplifiers, connected via 15 kΩ resistor to V_{DDA}.
V_{DDA4}	64	Analog supply voltage 4 for the Y/C/CVBS DACs.
n.c.	65	not connected
n.c.	66	not connected
V_{SSA}	67	Analog ground for the DACs.
$I_{Y/C/CVBS}$	68	Current input for the Y/C/CVBS amplifiers, connected via 15 kΩ resistor to V_{DDA}.
CHROMA	69	Analog output of the chrominance signal.
V_{DDA5}	70	Analog supply voltage 5 for the Y/C/CVBS DACs.
Y	71	Analog output of the luminance signal.
V_{DDA6}	72	Analog supply voltage 6 for the Y/C/CVBS DACs.
CVBS	73	Analog output of the CVBS signal.

SYMBOL	PIN	DESCRIPTION
V_{DDA7}	74	Analog supply voltage 6 for the Y/C/CVBS DACs.
V_{refH2}	75	Upper reference voltage 2 input for the Y/C/CVBS DACs, connected via 100 nF capacitor to $V_{SSA.}$
V_{refL2}	76	Lower reference voltage 2 input for the Y/C/CVBS DACs, connect to V_{SSA}.
AP	77	Test pin. Connected to digital ground for normal operation.
SP	78	Test pin. Connected to digital ground for normal operation.
V_{SSD8}	79	digital ground 8
V_{DDD8}	80	digital supply voltage 8
V_{SSD9}	81	digital ground 9
V_{DDD9}	82	digital supply voltage 9
SCL	83	I^2C-bus serial clock input.
SDA	84	I^2C-bus serial data input/output.

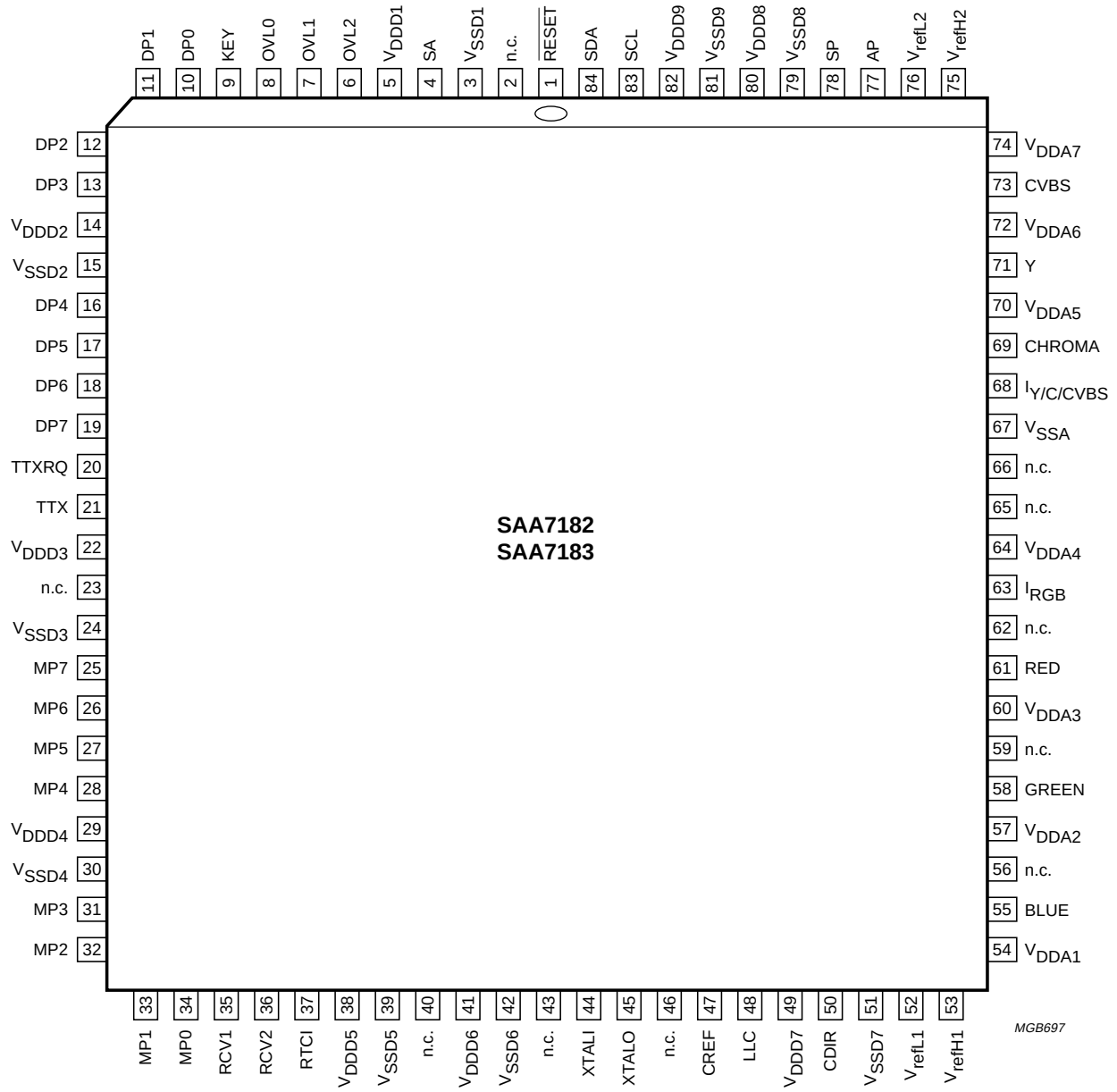


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The digital video encoder (EURO-DENC) encodes digital luminance and colour difference signals into analog CVBS and simultaneously S-Video signals. NTSC-M, PAL B/G and SECAM standards and sub-standards are supported.

Both interlaced and non-interlaced operation is possible for all standards.

In addition to RED, GREEN and BLUE converted components, the dematrixed YUV input is available on three separate analog outputs.

The basic encoder function consists of subcarrier generation and colour modulation also insertion of synchronization signals. Luminance and chrominance signals are filtered in accordance with the standard requirements of RS-170-A and *"CCIR 624"*.

For ease of analog post filtering the signals are twice oversampled with respect to the pixel clock before digital-to-analog conversion.

For total filter transfer characteristics see Figs 3, 4, 5, 6, 7 and 8. The DACs for Y, C and CVBS are realized with full 10-bit resolution, DACs for RGB are with 9-bit resolution.

The MPEG port (MP) accept 8 lines multiplexed Cb-Y-Cr data.

The 8-bit multiplexed Cb-Y-Cr formats are *"CCIR 656"* (D1 format) compatible, but the SAV, EAV etc. codes are not decoded.

Alternatively, 8-bits Y on MP port and 8-bit multiplexed Cb, Cr on DP port can be chosen as input.

A crystal-stable master clock (LLC) of 27 MHz, which is twice the CCIR line-locked pixel clock of 13.5 MHz, needs to be supplied externally. Optionally, a crystal oscillator input/output pair of pins and an on-chip clock driver is provided.

It is also possible to connect a Philips Digital Video Decoder (SAA7111 or SAA7151B) in conjunction with a CREF clock qualifier to EURO-DENC. Via RTCI pin connected to RTCO of a decoder, information concerning actual subcarrier, PAL-ID (see *"data sheet SAA7111"*) definite subcarrier phase can be inserted.

The EURO-DENC synthesizes all necessary internal signals, colour subcarrier frequency, and synchronization signals, from that clock. The encoder is always timing master for the MPEG port (MP), but it can additionally be configured as slave with respect to the RCV trigger inputs.

European teletext encoding is supported if an appropriate teletext bitstream is applied to the TTX pin.

The IC also contains Closed Caption and Extended Data Services Encoding (Line 21), and supports anti-taping signal generation in accordance with Macrovision; it also supports overlay via KEY and three control bits by a 24×8 LUT.

A number of possibilities are provided for setting of different video parameters such as:

- Black and blanking level control
- Colour subcarrier frequency
- Variable burst amplitude etc.

During reset ($\overline{\text{RESET}}$ = LOW) and after reset is released, all digital I/O stages are set to input mode. A reset forces the I^2C-bus interface to abort any running bus transfer and sets register 3A to 03H, register 61 to 06H and registers 6BH and 6EH to 00H. All other control registers are not influenced by a reset.

Data manager

In the data manager, real time arbitration on the data stream to be encoded is performed.

Depending on the polarity of pin KEY, the MP input (or MP/DP input) or OVL input are selected to be encoded to CVBS and Y/C signals, and output as RGB.

KEY controls OVL entries of a programmable LUT for encoded signals and for RGB output. The common KEY switching signal can be disabled by software for the signals to be encoded (Y, C and CVBS), such that OVL will appear on RGB outputs, but not on Y, C and CVBS.

OVL input under control of KEY can be also used to insert decoded teletext information or other on-screen data.

Optionally, the OVL colour LUTs located in this block, can be read out in a pre-defined sequence (8 steps per active video line), achieving, for example, a colour bar test pattern generator without need for an external data source. The colour bar function is only under software control.

Encoder

VIDEO PATH

The encoder generates out of Y, U and V baseband signals luminance and colour subcarrier output signals, suitable for use as CVBS or separate Y and C signals.

Luminance is modified in gain and in offset (latter programmable in a certain range to enable different black level set-ups). After having been inserted a fixed synchronization level, in accordance with standard composite synchronization schemes, and blanking level, programmable also in a certain range to allow for manipulations with Macrovision anti-taping, additional insertion of AGC super-white pulses, programmable in height, is supported.

In order to enable easy analog post filtering, luminance is interpolated from 13.5 MHz data rate to 27 MHz data rate, providing luminance in 10-bit resolution. This filter is also used to define smoothed transients for synchronization pulses and blanking period. For transfer characteristic of the luminance interpolation filter see Figs 5 and 6.

Chrominance is modified in gain (programmable separately for U and V), standard dependent burst is inserted, before baseband colour signals are interpolated from 6.75 MHz data rate to 27 MHz data rate. One of the interpolation stages can be bypassed, thus providing a higher colour bandwidth, which can be made use of for Y/C output. For transfer characteristics of the chrominance interpolation filter see Figs 3 and 4.

The amplitude of inserted burst is programmable in a certain range, suitable for standard signals and for special effects. Behind the succeeding quadrature modulator, colour in 10-bit resolution is provided on subcarrier.

The numeric ratio between Y and C outputs is in accordance with set standards.

TELETEXT INSERTION AND ENCODING

Pin TTX receives a teletext bitstream sampled at the LLC clock, each teletext bit is carried by four or three LLC samples.

Phase variant interpolation is achieved on this bitstream in the internal teletext encoder, providing sufficient small phase jitter on the output text lines.

TTXRQ provides a fully programmable request signal to the teletext source, indicating the insertion period of bitstream at lines selectable independently for both fields. The internal insertion window for text is set to 360 teletext bits including clock run-in bits. For protocol and timing see Fig.17.

CLOSED CAPTION ENCODER

Using this circuit, data in accordance with the specification of Closed Caption or Extended Data Service, delivered by the control interface, can be encoded (Line 21). Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number where data is to be encoded in, can be modified in a certain range.

Data clock frequency is in accordance with definition for NTSC-M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode Closed Caption Data for 50 Hz field frequencies at 32 times horizontal line frequency.

ANTI-TAPING (SAA7183 ONLY)

For more information contact your nearest Philips Semiconductors sales office.

RGB processor

This block contains a dematrix in order to produce RED, GREEN and BLUE signals to be fed to a SCART plug.

Before Y, Cb, Cr signals are dematrixed, 2 times oversampling for luminance and 4 times oversampling for colour difference signals is performed. For transfer curves of luminance and colour difference components of RGB see Figs 7 and 8.

SECAM processor

SECAM specific pre-processing is achieved in this block by a pre-emphasis of colour difference signals (for gain and phase see Figs 9 and 10.

A baseband frequency modulator with a reference frequency shifted from 4.286 MHz to DC carries out SECAM modulation in accordance with appropriate standard or optionally wide clipping limits.

After the HF pre-emphasis, also applied on a DC reference carrier (anti-Cloche filter; see Figs 11 and 12), line-by-line sequential carriers with black reference of 4.25 MHz (Db) and 4.40625 MHz (Dr) are generated using specified values for FSC programming bytes.

Alternating phase reset in accordance with SECAM standard is carried out automatically. During vertical blanking the so-called bottle pulses are not provided.

Output interface/DACs

In the output interface encoded both Y and C signals are converted from digital-to-analog in 10-bit resolution. Y and C signals are also combined to a 10-bit CVBS signal.

The CVBS output occurs with the same processing delay as the Y and C outputs. Absolute amplitudes at the input of the DAC for CVBS is reduced by $^{15}/_{16}$ with respect to Y and C DACs to make maximum use of conversion ranges.

RED, GREEN and BLUE signals are also converted from digital-to-analog, each providing a 9-bit resolution.

Outputs of the DACs can be set together in two groups via software control to minimum output voltage for either purpose.

Synchronization

Synchronization of the EURO-DENC is able to operate in two modes; slave mode and master mode.

In the slave mode, the circuit accepts synchronization pulses at the bidirectional RCV1 port. The timing and trigger behaviour related to RCV1 can be influenced by programming the polarity and on-chip delay of RCV1. Active slope of RCV1 defines the vertical phase and optionally the odd/even and colour frame phase to be initialized, it can be also used to set the horizontal phase.

If the horizontal phase is not be influenced by RCV1, a horizontal pulse needs to be supplied at the RCV2 pin. Timing and trigger behaviour can also be influenced for RCV2.

If there are missing pulses at RCV1 and/or RCV2, the time base of EURO-DENC runs free, thus an arbitrary number of synchronization slopes may miss, but no additional pulses (such with wrong phase) must occur.

If the vertical and horizontal phase is derived from RCV1, RCV2 can be used for horizontal or composite blanking input or output.

In the master mode, the time base of the circuit continuously runs free. On the RCV1 port, the IC can output:

- A Vertical Sync signal (VS) with 3 or 2.5 lines duration, or
- An ODD/EVEN signal which is LOW in odd fields, or
- A field sequence signal (FSEQ) which is HIGH in the first of 4 respectively 8 respectively 12 fields.

On the RCV2 port, the IC can provide a horizontal pulse with programmable start and stop phase; this pulse can be inhibited in the vertical blanking period to build up, for example, a composite blanking signal.

The polarity of both RCV1 and RCV2 is selectable by software control.

Field length is in accordance with 50 Hz or 60 Hz standards, including non-interlaced options; start and end of its active part can be programmed. The active part of a field always starts at the beginning of a line, if the standard blanking option SBLBN is not set.

I²C-bus interface

The I²C-bus interface is a standard slave transceiver, supporting 7-bit slave addresses and 400 kbits/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write only, except one readable status byte.

Two I²C-bus slave addresses are selected:

88H: LOW at pin 4

8CH: HIGH at pin 4.

Input levels and formats

EURO-DENC expects digital Y, Cb, Cr data with levels (digital codes) in accordance with *“CCIR 601”*.

For C and CVBS outputs, deviating amplitudes of the colour difference signals can be compensated by independent gain control setting, while gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

For RGB outputs fixed amplification in accordance with *“CCIR 601”* is provided.

Reference levels are measured with a colour bar, 100% white, 100% amplitude and 100% saturation.

Table 1 *"CCIR 601"* signal component levels

COLOUR	SIGNALS[1]					
	Y	Cb	Cr	R[2]	G[2]	B[2]
White	235	128	128	235	235	235
Yellow	210	16	146	235	235	16
Cyan	170	166	16	16	235	235
Green	145	54	34	16	235	16
Magenta	106	202	222	235	16	235
Red	81	90	240	235	16	16
Blue	41	240	110	16	16	235
Black	16	128	128	16	16	16

Notes

1. Transformation:
   a) $R = Y + 1.3707 \times (Cr - 128)$
   b) $G = Y - 0.3365 \times (Cb - 128) - 0.6982 \times (Cb - 128)$
   c) $B = Y + 1.7324 \times (Cb - 128)$.
2. Representation of R, G and B at the output is 9 bits at 27 MHz.

Table 2 8-bit multiplexed format (similar to *"CCIR 601"*)

TIME	0	1	2	2	4	5	6	7
Sample	Cb_0	Y_0	Cr_0	Y_1	Cb_2	Y_2	Cr_2	Y_3
Luminance pixel number	0		1		2		3	
Colour pixel number	0				2			

Table 3 16-bit multiplexed format (DTV2 format)

TIME	0	1	2	3	4	5	6	7
Sample Y line	Y_0		Y_1		Y_2		Y_3	
Sample UV line	Cb_0		Cr_0		Cb_2		Cr_2	
Luminance pixel number	0		1		2		3	
Colour pixel number	0				2			

Bit allocation map

Table 4 Slave Receiver (Slave Address 88H or 8CH)

REGISTER FUNCTION	SUB ADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Null	00	0	0	0	0	0	0	0	0
	↓	↓							
Null	39	0	0	0	0	0	0	0	0
Input port control	3A	CBENB	DISKEY	0	0	0	FMT16	Y2C	UV2C
OVL LUT Y0	42	OVLY07	OVLY06	OVLY05	OVLY04	OVLY03	OVLY02	OVLY01	OVLY00
OVL LUT U0	43	OVLU07	OVLU06	OVLU05	OVLU04	OVLU03	OVLU02	OVLU01	OVLU00
OVL LUT V0	44	OVLV07	OVLV06	OVLV05	OVLV04	OVLV03	OVLV02	OVLV01	OVLV00
	↓	↓							
OVL LUT Y7	57	OVLY77	OVLY76	OVLY75	OVLY74	OVLY73	OVLY72	OVLY71	OVLY70
OVL LUT U7	58	OVLU77	OVLU76	OVLU75	OVLU74	OVLU73	OVLU72	OVLU71	OVLU70
OVL LUT V7	59	OVLV77	OVLV76	OVLV75	OVLV74	OVLV73	OVLV72	OVLV71	OVLV70
Chrominance phase	5A	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0
Gain U	5B	GAINU7	GAINU6	GAINU5	GAINU4	GAINU3	GAINU2	GAINU1	GAINU0
Gain V	5C	GAINV7	GAINV6	GAINV5	GAINV4	GAINV3	GAINV2	GAINV1	GAINV0
Gain U MSB, black level	5D	GAINU8	0	BLCKL5	BLCKL4	BLCKL3	BLCKL2	BLCKL1	BLCKL0
Gain V MSB, blanking level, decoder type	5E	GAINV8	DECTYP	BLNNL5	BLNNL4	BLNNL3	BLNNL2	BLNNL1	BLNNL0
Blanking level VBI	5F	0	0	BLNVB5	BLNVB4	BLNVB3	BLNVB2	BLNVB1	BLNVB0
Null	60	0	0	0	0	0	0	0	0
Standard control	61	DOWNB	DOWNA	INPI	YGS	SECAM	SCBW	PAL	FISE
Burst amplitude	62	RTCE	BSTA6	BSTA5	BSTA4	BSTA3	BSTA2	BSTA1	BSTA0
Subcarrier 0	63	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
Subcarrier 1	64	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
Subcarrier 2	65	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
Subcarrier 3	66	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
Line 21 odd 0	67	L21O07	L21O06	L21O05	L21O04	L21O03	L21O02	L21O01	L21O00
Line 21 odd 1	68	L21O17	L21O16	L21O15	L21O14	L21O13	L21O12	L21O11	L21O10
Line 21 even 0	69	L21E07	L21E06	L21E05	L21E04	L21E03	L21E02	L21E01	L21E00
Line 21 even 1	6A	L21E17	L21E16	L21E15	L21E14	L21E13	L21E12	L21E11	L21E10

REGISTER FUNCTION	SUB ADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
RCV port control	6B	SRCV11	SRCV10	TRCV2	ORCV1	PRCV1	CBLF	ORCV2	PRCV2
Trigger control	6C	HTRIG7	HTRIG6	HTRIG5	HTRIG4	HTRIG3	HTRIG2	HTRIG1	HTRIG0
Trigger control	6D	HTRIG10	HTRIG9	HTRIG8	VTRIG4	VTRIG3	VTRIG2	VTRIG1	VTRIG0
Multi control	6E	SBLBN	0	PHRES1	PHRES0	0	0	FLC1	FLC0
Closed caption/teletext control	6F	CCEN1	CCEN0	TTXEN	SCCLN4	SCCLN3	SCCLN2	SCCLN1	SCCLN0
RCV2 output start	70	RCV2S7	RCV2S6	RCV2S5	RCV2S4	RCV2S3	RCV2S2	RCV2S1	RCV2S0
RCV2 output end	71	RCV2E7	RCV2E6	RCV2E5	RCV2E4	RCV2E3	RCV2E2	RCV2E1	RCV2E0
MSBs RCV2 output	72	0	RCV2E10	RCV2E9	RCV2E8	0	RCV2S10	RCV2S9	RCV2S8
TTX request H start	73	TTXHS7	TTXHS6	TTXHS5	TTXHS4	TTXHS3	TTXHS2	TTXHS1	TTXHS0
TTX request H end	74	TTXHE7	TTXHE6	TTXHE5	TTXHE4	TTXHE3	TTXHE2	TTXHE1	TTXHE0
MSBs TTX request H	75	0	TTXHE10	TTXHE9	TTXHE8	0	TTXHS10	TTXHS9	TTXHS8
TTX odd request V S	76	TTXOVS7	TTXOVS6	TTXOVS5	TTXOVS4	TTXOVS3	TTXOVS2	TTXOVS1	TTXOVS0
TTX odd request V E	77	TTXOVE7	TTXOVE6	TTXOVE5	TTXOVE4	TTXOVE3	TTXOVE2	TTXOVE1	TTXOVE0
TTX even request V S	78	TTXEVS7	TTXEVS6	TTXEVS5	TTXEVS4	TTXEVS3	TTXEVS2	TTXEVS1	TTXEVS0
TTX even request V E	79	TTXEVE7	TTXEVE6	TTXEVE5	TTXEVE4	TTXEVE3	TTXEVE2	TTXEVE1	TTXEVE0
First active line	7A	FAL7	FAL6	FAL5	FAL4	FAL3	FAL2	FAL1	FAL0
Last active line	7B	LAL7	LAL6	LAL5	LAL4	LAL3	LAL2	LAL1	LAL0
MSBs vertical	7C	0	LAL8	0	FAL8	TTXEVE8	TTXOVE8	TTXEVS8	TTXOVS8
Null	7D	0	0	0	0	0	0	0	0
Null	7E	0	0	0	0	0	0	0	0
Null	7F	0	0	0	0	0	0	0	0

I²C-bus format

Table 5 I²C-bus address; see Table 6

S	SLAVE ADDRESS	ACK	SUBADDRESS	ACK	DATA 0	ACK	--------	DATA n	ACK	P

Table 6 Explanation of Table 5

PART	DESCRIPTION
S	START condition
Slave address	1 0 0 0 1 0 0 X or 1 0 0 0 1 1 0 X (note 1)
ACK	acknowledge, generated by the slave
Subaddress (note 2)	subaddress byte
DATA	data byte
--------	continued data bytes and ACKs
P	STOP condition

Notes

1. X is the read/write control bit; X = logic 0 is order to write; X = logic 1 is order to read, no subaddressing with read.
2. If more than 1 byte DATA is transmitted, then auto-increment of the subaddress is performed.

Slave Receiver

Table 7 Subaddress 3A

DATA BYTE	LOGIC LEVEL	DESCRIPTION
UV2C	0	Cb/Cr data are two's complement.
	1	Cb/Cr data are straight binary. Default after reset.
Y2C	0	Y data are two's complement.
	1	Y data are straight binary. Default after reset.
FMT16	0	Selects Cb, Y, Cr, Y on 8 lines on MP port (*"CCIR 656"* compatible). Default after reset.
	1	Selects Cb, Cr on DP port and Y on MP port.
DISKEY	0	OVL keying enabled for Y, C and CVBS outputs. Default after reset.
	1	OVL keying disabled for Y, C and CVBS outputs.
CBENB	0	Data from input ports are encoded. Default after reset.
	1	Colour bar with programmable colours (entries of OVL_LUTs) is encoded. The LUTs are read in upward order from index 0 to index 7.

Table 8 Subaddress 42 to 59

COLOUR	DATA BYTE (note 1)			INDEX (note 2)
	OVLY	OVLU	OVLV	
White	107 (6BH)	0 (00H)	0 (00H)	0
	107 (6BH)	0 (00H)	0 (00H)	
Yellow	82 (52H)	144 (90H)	18 (12H)	1
	34 (22H)	172 (ACH)	14 (0EH)	
Cyan	42 (2AH)	38 (26H)	144 (90H)	2
	03 (03H)	29 (1DH)	172 (ACH)	
Green	17 (11H)	182 (B6H)	162 (A2H)	3
	240 (F0H)	200 (C8H)	185 (B9H)	
Magenta	234 (EAH)	74 (4AH)	94 (5EH)	4
	212 (D4H)	56 (38H)	71 (47H)	
Red	209 (D1H)	218 (DAH)	112 (70H)	5
	193 (C1H)	227 (E3H)	84 (54H)	
Blue	169 (A9H)	112 (70H)	238 (EEH)	6
	163 (A3H)	84 (54H)	242 (F2H)	
Black	144 (90H)	0 (00H)	0 (00H)	7
	144 (90H)	0 (00H)	0 (00H)	

Notes

1. Contents of OVL look-up tables. All 8 entries are 8-bits. Data representation is in accordance with *"CCIR 601"* (Y, Cb, Cr), but two's complement, e.g. for a $^{100}/_{100}$ (upper number) or $^{100}/_{75}$ (lower number) colour bar.
2. For normal colour bar with CBENB = logic 1.

Table 9 Subaddress 5A

DATA BYTE(1)	VALUE	RESULT
CHPS	68H	PAL-B/G and data from input ports
	92H	PAL-B/G and data from look-up table
	82H	NTSC-M and data from input ports
	A4H	NTSC-M and data from look-up table

Note

1. Phase of encoded colour subcarrier (including burst) relative to horizontal sync. Can be adjusted in steps of 360/256 degrees.

Table 10 Subaddress 5B and 5D

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINU	variable gain for Cb signal; input representation accordance with *"CCIR 601"*	white-to-black = 92.5 IRE(1)	
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 118 (76H)	output subcarrier of U contribution = nominal
		white-to-black = 100 IRE(2)	
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 125 (7DH)	output subcarrier of U contribution = nominal
	nominal GAINU for SECAM encoding	value = 106 (6AH)	

Notes

1. GAINU = –2.17 × nominal to +2.16 × nominal.
2. GAINU = –2.05 × nominal to +2.04 × nominal.

Table 11 Subaddress 5C and 5E

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINV	variable gain for Cr signal; input representation accordance with *"CCIR 601"*	white-to-black = 92.5 IRE(1)	
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 165 (A5H)	output subcarrier of V contribution = nominal
		white-to-black = 100 IRE(2)	
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 175 (AFH)	output subcarrier of V contribution = nominal
	nominal GAINV for SECAM encoding	value = –129 (17FH)	

Notes

1. GAINV = –1.55 × nominal to +1.55 × nominal.
2. GAINV = –1.46 × nominal to +1.46 × nominal.

Table 12 Subaddress 5D

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLCKL	variable black level; input representation accordance with *"CCIR 601"*	white-to-sync = 140 IRE(1)	
		BLCKL = 0	output black level = 24 IRE
		BLCKL = 63 (3FH)	output black level = 49 IRE
		white-to-sync = 143 IRE(2)	
		BLCKL = 0	output black level = 24 IRE
		BLCKL = 63 (3FH)	output black level = 50 IRE

Notes

1. Output black level/IRE = BLCKL × 25/63 + 24; recommended value: BLCKL = 60 (3CH) normal.
2. Output black level/IRE = BLCKL × 26/63 + 24; recommended value: BLCKL = 45 (2DH) normal.

Table 13 Subaddress 5E

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLNNL	variable blanking level	white-to-sync = 140 IRE[1]	
		BLNNL = 0	output blanking level = 17 IRE
		BLNNL = 63 (3FH)	output blanking level = 42 IRE
		white-to-sync = 143 IRE[2]	
		BLNNL = 0	output blanking level = 17 IRE
		BLNNL = 63 (3FH)	output blanking level = 43 IRE
DECTYP	RTCI	logic 0	real time control input from SAA7151B
		logic 1	real time control input from SAA7111

Notes

1. Output black level/IRE = BLNNL × 25/63 + 17; recommended value: BLNNL = 58 (3AH) normal.
2. Output black level/IRE = BLNNL × 26/63 + 17; recommended value: BLNNL = 63 (3FH) normal.

Table 14 Subaddress 5F

DATA BYTE	DESCRIPTION
BLNVB	variable blanking level during vertical blanking interval is typically identical to value of BLNNL

Table 15 Subaddress 61:

DATA BYTE	LOGIC LEVEL	DESCRIPTION
FISE	0	864 total pixel clocks per line; default after reset
	1	858 total pixel clocks per line
PAL	0	NTSC encoding (non-alternating V component)
	1	PAL encoding (alternating V component); default after reset
SCBW	0	enlarged bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 3 and 4); wide clipping for SECAM
	1	standard bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 3 and 4); default after reset
SECAM	0	no SECAM encoding; default after reset
	1	SECAM encoding activated
YGS	0	luminance gain for white – black 100 IRE; default after reset
	1	luminance gain for white – black 92.5 IRE including 7.5 IRE set-up of black
INPI	0	PAL switch phase is nominal; default after reset
	1	PAL switch phase is inverted compared to nominal
DOWNA	0	DACs for CVBS, Y and C in normal operational mode; default after reset
	1	DACs for CVBS, Y and C forced to lowest output voltage
DOWNB	0	DACs for R, G and B in normal operational mode; default after reset
	1	DACs for R, G and B forced to lowest output voltage

Table 16 Subaddress 62A

DATA BYTE	LOGIC LEVEL	DESCRIPTION
RTCE	0	no real time control of generated subcarrier frequency
	1	real time control of generated subcarrier frequency through SAA7151B or SAA7111 (timing see Fig.16)

Table 17 Subaddress 62B

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BSTA	amplitude of colour burst; input representation in accordance with *"CCIR 601"*	white-to-black = 92.5 IRE; burst = 40 IRE; NTSC encoding BSTA = 0 to 1.25 × nominal(1) white-to-black = 92.5 IRE; burst = 40 IRE; PAL encoding BSTA = 0 to 1.76 × nominal(2) white-to-black = 100 IRE; burst = 43 IRE; NTSC encoding BSTA = 0 to 1.20 × nominal(3) white-to-black = 100 IRE; burst = 43 IRE; PAL encoding BSTA = 0 to 1.67 × nominal(4)	
	fixed burst amplitude with SECAM encoding		

Notes

1. Recommended value: BSTA = 102 (66H).
2. Recommended value: BSTA = 72 (48H).
3. Recommended value: BSTA = 106 (6AH).
4. Recommended value: BSTA = 75 (4BH).

Table 18 Subaddress 63 to 66 (four bytes to program subcarrier frequency)

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
FSC0 to FSC3	f_{fsc} = subcarrier frequency (in multiples of line frequency); f_{llc} = clock frequency (in multiples of line frequency)	$FSC = round\left(\frac{f_{fsc}}{f_{llc}} \times 2^{32}\right)$ see note 1	FSC3 = most significant byte FSC0 = least significant byte

Note

1. Examples:
   a) NTSC-M: f_{fsc} = 227.5, f_{llc} = 1716 → FSC = 569408543 (21F07C1FH).
   b) PAL-B/G: f_{fsc} = 283.7516, f_{llc} = 1728 → FSC = 705268427 (2A098ACBH).
   c) SECAM: f_{fsc} = 274.304, f_{llc} = 1728 → FSC = 681786290 (28A33BB2H).

Table 19 Subaddress 67 to 6A

DATA BYTE[1]	DESCRIPTION
L21O0	first byte of captioning data, odd field
L21O1	second byte of captioning data, odd field
L21E0	first byte of extended data, even field
L21E1	second byte of extended data, even field

Note

1. LSBs of the respective bytes are encoded immediately after run-in and framing code, the MSBs of the respective bytes have to carry the parity bit, in accordance with the definition of Line 21 encoding format.

Table 20 Subaddress 6B

DATA BYTE	LOGIC LEVEL	DESCRIPTION
PRCV2	0	polarity of RCV2 as output is active HIGH, rising edge is taken when input; default after reset
	1	polarity of RCV2 as output is active LOW, falling edge is taken when input
ORCV2	0	pin RCV2 is switched to input; default after reset
	1	pin RCV2 is switched to output
CBLF	0	if ORCV2 = HIGH, pin RCV2 provides an HREF signal (Horizontal Reference Pulse that is defined by RCV2S and RCV2E, also during vertical blanking Interval); default after reset if ORCV2 = LOW, signal input to RCV2 is used for horizontal synchronization only (if TRCV2 = 1); default after reset
	1	if ORCV2 = HIGH, pin RCV2 provides a ‘Composite-Blanking-Not’ signal, for example a reference pulse that is defined by RCV2S and RCV2E, excluding Vertical Blanking Interval, which is defined by FAL and LAL (PRCV2 must be LOW) if ORCV2 = LOW, signal input to RCV2 is used for horizontal synchronization (if TRCV2 = 1) and as an internal blanking signal
PRCV1	0	polarity of RCV1 as output is active HIGH, rising edge is taken when input, respectively; default after reset
	1	polarity of RCV1 as output is active LOW, falling edge is taken when input, respectively
ORCV1	0	pin RCV1 is switched to input; default after reset
	1	pin RCV1 is switched to output
TRCV2	0	horizontal synchronization is taken from RCV1 port; default after reset
	1	horizontal synchronization is taken from RCV2 port
SRCV1	–	defines signal type on pin RCV1; see Table 21

Table 21 Logic levels and function of SRCV1

DATA BYTE		AS OUTPUT	AS INPUT	FUNCTION
SRCV11	SRCV10			
0	0	VS	VS	vertical sync each field; default after reset
0	1	FS	FS	frame sync (odd/even)
1	0	FSEQ	FSEQ	field sequence, vertical sync every fourth field (PAL = SECAM = 0), eighth field (PAL = 1) or twelfth field (SECAM = 1)
1	1	not applicable	not applicable	–

Table 22 Subaddress 6C, 6D

DATA BYTE	DESCRIPTION
HTRIG	sets the horizontal trigger phase related to signal on RCV1 or RCV2 input values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed increasing HTRIG decreases delays of all internally generated timing signals reference mark: analog output horizontal sync (leading slope) coincides with active edge of RCV used for triggering at HTRIG = 049H (054H)

Table 23 Subaddress 6D

DATA BYTE	LOGIC LEVEL	DESCRIPTION
VTRIG	–	sets the vertical trigger phase related to signal on RCV1 input increasing VTRIG decreases delays of all internally generated timing signals, measured in half lines variation range of VTRIG = 0 to 31 (1FH)

Table 24 Subaddress 6E

DATA BYTE	LOGIC LEVEL	DESCRIPTION
SBLBN	0	vertical blanking is defined by programming of FAL and LAL; default after reset
	1	vertical blanking is forced in accordance with *"CCIR 624"* (50 Hz) or RS170A (60 Hz)
PHRES	–	selects the phase reset mode of the colour subcarrier generator; see Table 25
FLC	–	field length control; see Table 26

Table 25 Logic levels and function of PHRES

DATA BYTE		FUNCTION
PHRES1	PHRES0	
0	0	no reset or reset via RTCI from SAA7111 if bit RTCE = 1; default after reset
0	1	reset every two lines or SECAM-specific if bit SECAM = 1
1	0	reset every eight fields
1	1	reset every four fields

Table 26 Logic levels and function of FLC

DATA BYTE		FUNCTION
FLC1	FLC0	
0	0	interlaced 312.5 lines/field at 50 Hz, 262.5 lines/field at 60 Hz; default after reset
0	1	non-interlaced 312 lines/field at 50 Hz, 262 lines/field at 60 Hz
1	0	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz
1	1	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz

Table 27 Subaddress 6F

DATA BYTE	LOGIC LEVEL	DESCRIPTION
CCEN	–	enables individual line 21 encoding; see Table 28
TTXEN	0	disables teletext insertion
	1	enables teletext insertion
SCCLN	–	selects the actual line, where closed caption or extended data are encoded line = (SCCLN + 4) for M-systems line = (SCCLN + 1) for other systems

Table 28 Logic levels and function of CCEN

DATA BYTE		FUNCTION
CCEN1	CCEN0	
0	0	Line 21 encoding off
0	1	enables encoding in field 1 (odd)
1	0	enables encoding in field 2 (even)
1	1	enables encoding in both fields

Table 29 Subaddress 70 to 72

DATA BYTE	DESCRIPTION
RCV2S	start of output signal on RCV2 pin values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed first active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at RCV2S = 0F2H (110H)
RCV2E	end of output signal on RCV2 pin values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed last active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at RCV2E = 67CH (68AH)

Table 30 Subaddress 73 to 75

DATA BYTE	DESCRIPTION
TTXHS	start of signal on pin TTXRQ (standard for 50 Hz field rate = 13FH) values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed
TTXHE	end of signal on pin TTXRQ (standard for 50 Hz field rate = TTXHS + 1402 = 6B9H) values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed

Table 31 Subaddress 76, 77 and 7C

DATA BYTE	DESCRIPTION
TTXOVS	first line of occurrence of signal on pin TTXRQ in odd field
TTXOVE	last line of occurrence of signal on pin TTXRQ in odd field

Table 32 Subaddress 78, 79 and 7C

DATA BYTE	DESCRIPTION
TTXEVS	first line of occurrence of signal on pin TTXRQ in even field
TTXEVE	last line of occurrence of signal on pin TTXRQ in even field

Table 33 Subaddress 7A to 7C

DATA BYTE	DESCRIPTION
FAL	first active line = FAL + 4 for M-systems, = FAL + 1 for other systems, measured in lines FAL = 0 coincides with the first field synchronization pulse
LAL	last active line = LAL + 3 for M-systems, = LAL for other system, measured in lines LAL = 0 coincides with the first field synchronization pulse

SUBADDRESSES

In subaddresses 5B, 5C, 5D, 5E and 62 all IRE values are rounded up.

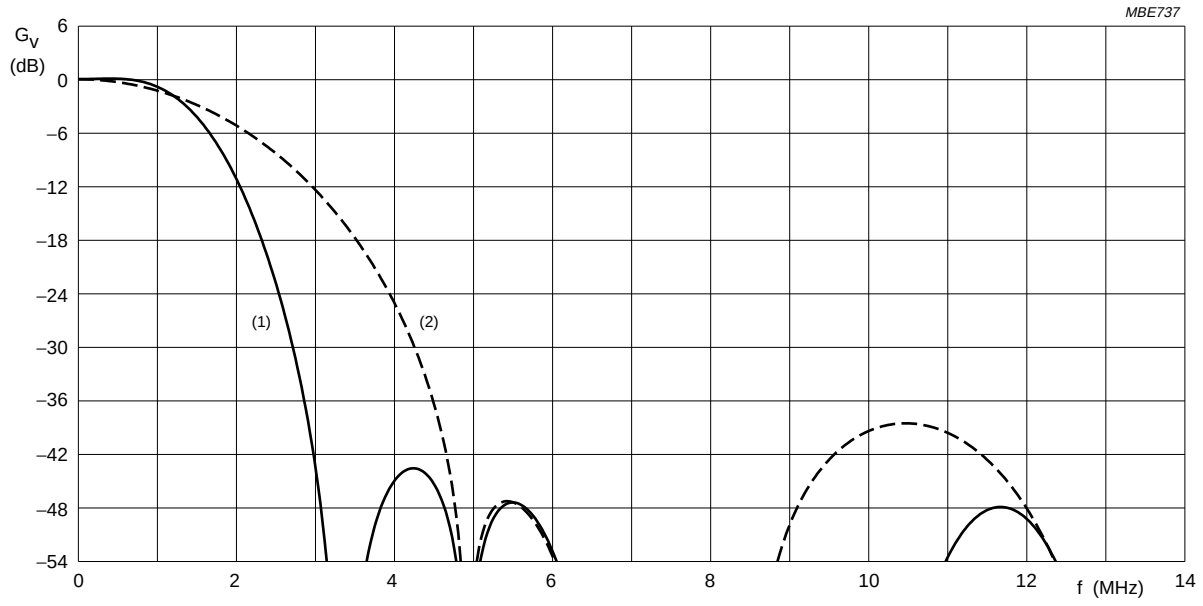
Slave Transmitter

Table 34 Slave transmitter (slave address 89H or 8DH)

REGISTER FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte	–	VER2	VER1	VER0	CCRDO	CCRDE	0	FSEQ	O_E

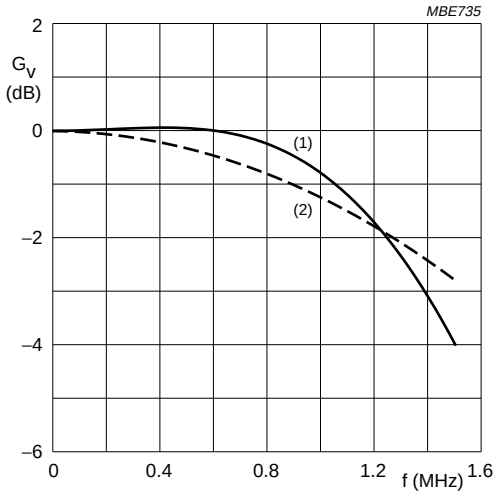
Table 35 No subaddress

DATA BYTE	LOGIC LEVEL	DESCRIPTION
VER	–	Version identification of the device. It will be changed with all versions of the IC that have different programming models. Current Version is 000 binary.
CCRDO	1	Closed caption bytes of the odd field have been encoded.
	0	The bit is reset after information has been written to the subaddresses 67 and 68. It is set immediately after the data has been encoded.
CCRDE	1	Closed caption bytes of the even field have been encoded.
	0	The bit is reset after information has been written to the subaddresses 69 and 6A. It is set immediately after the data has been encoded.
FSEQ	0	Not first field of a sequence.
	1	During first field of a sequence (repetition rate: NTSC = 4 fields, PAL = 8 fields, SECAM = 12 fields.
O_E	0	During odd field.
	1	During even field.



(1) SCBW = 1.
(2) SCBW = 0.

Fig.3 Chrominance transfer characteristic 1.



(1) SCBW = 1.
(2) SCBW = 0.

Fig.4 Chrominance transfer characteristic 2.

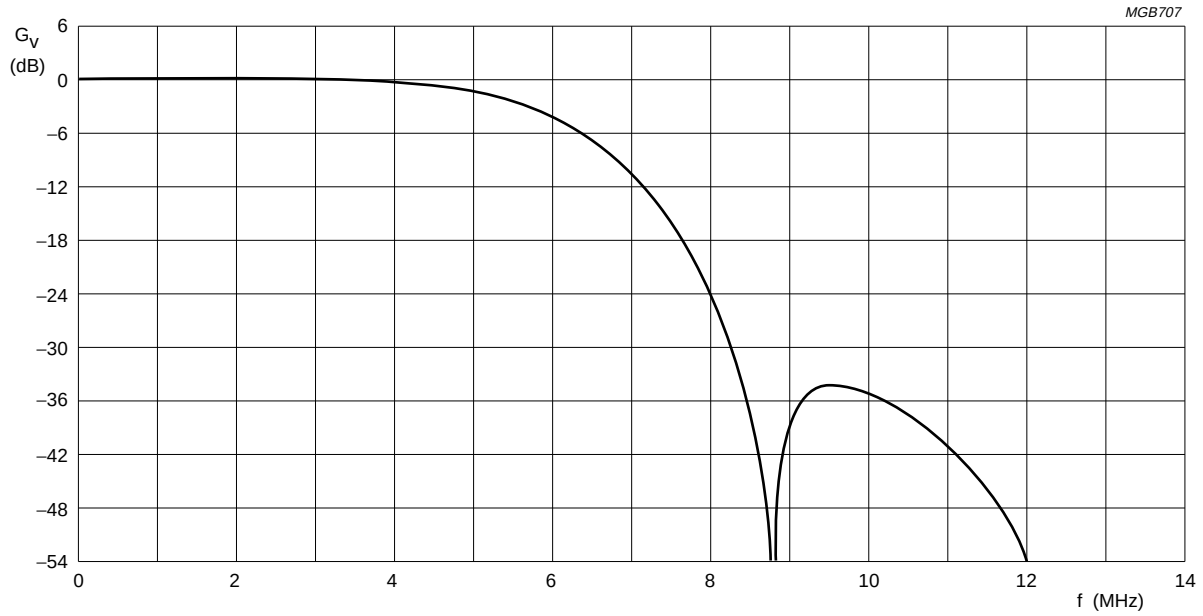


Fig.5 Total luminance of Y and CVBS; luminance transfer characteristic 1.

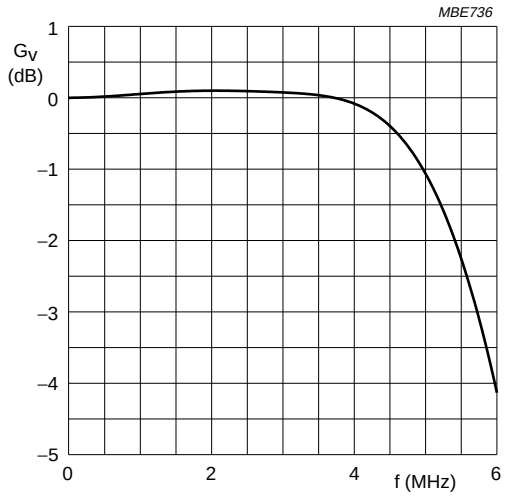


Fig.6 Detailed luminance of Y and CVBS; luminance transfer characteristic 2.

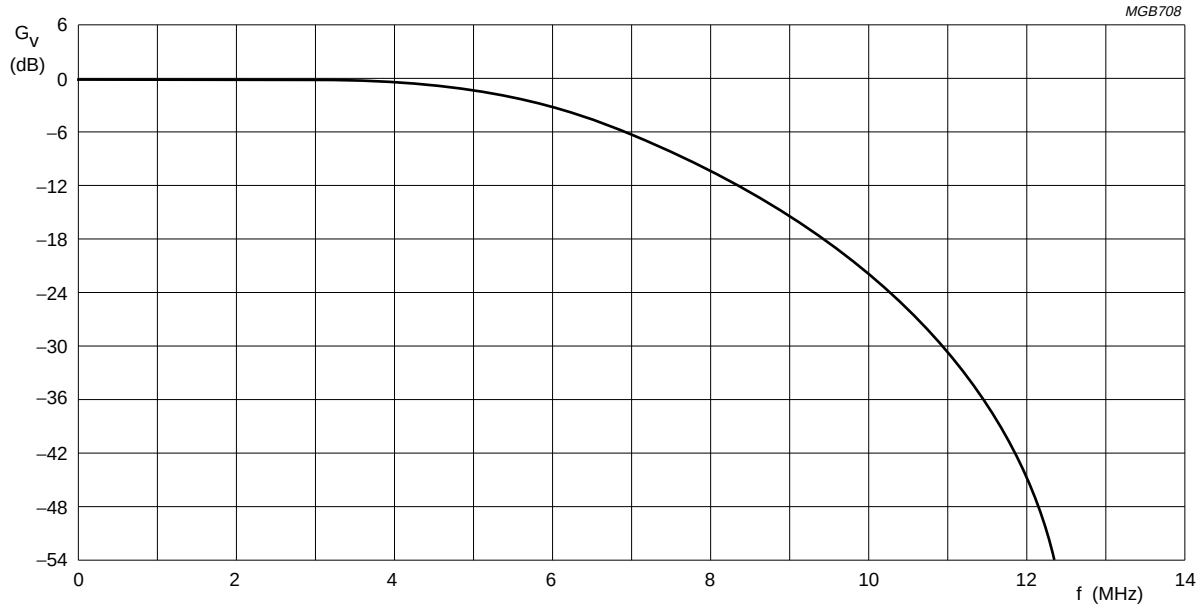


Fig.7 Luminance transfer characteristic in RGB.

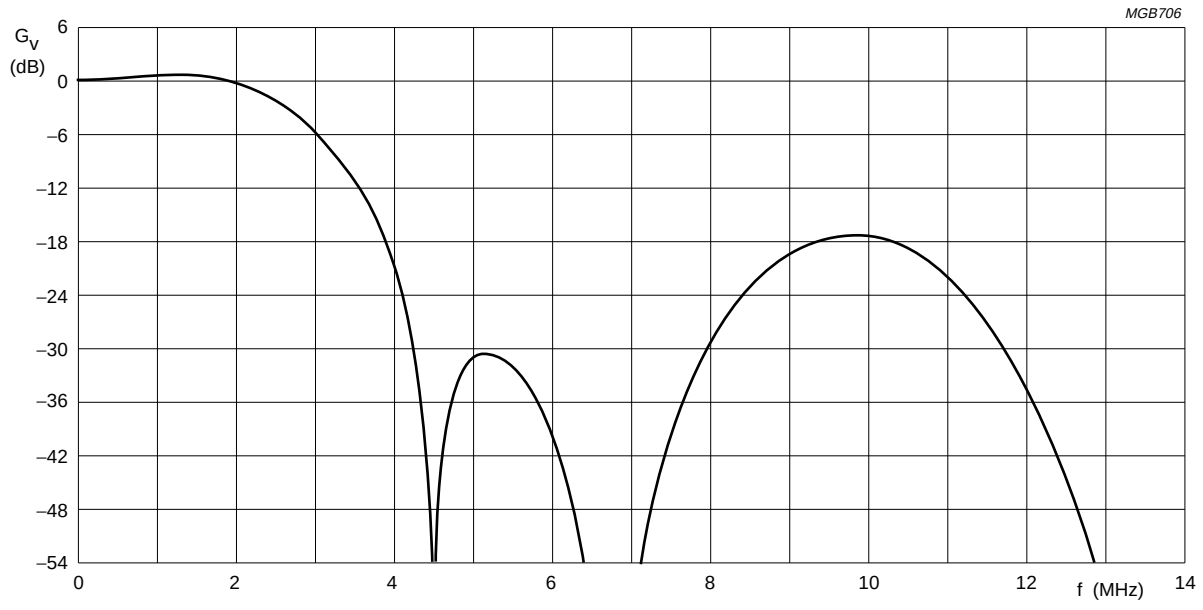


Fig.8 Colour difference transfer characteristic in RGB.

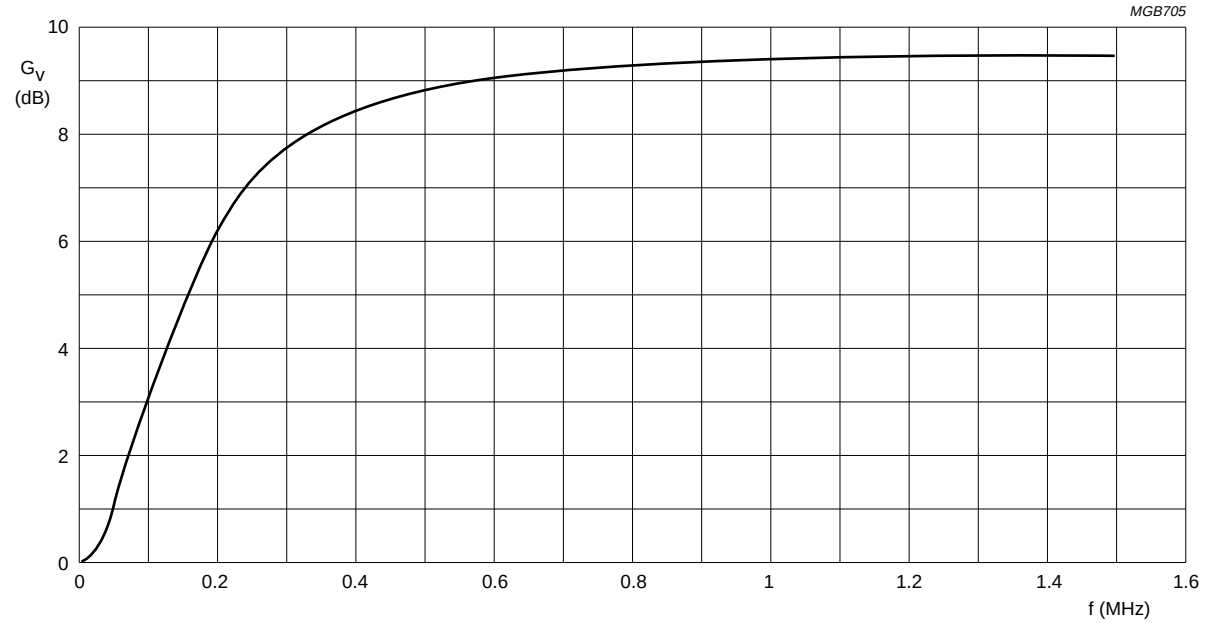


Fig.9 Gain of SECAM pre-emphasis.

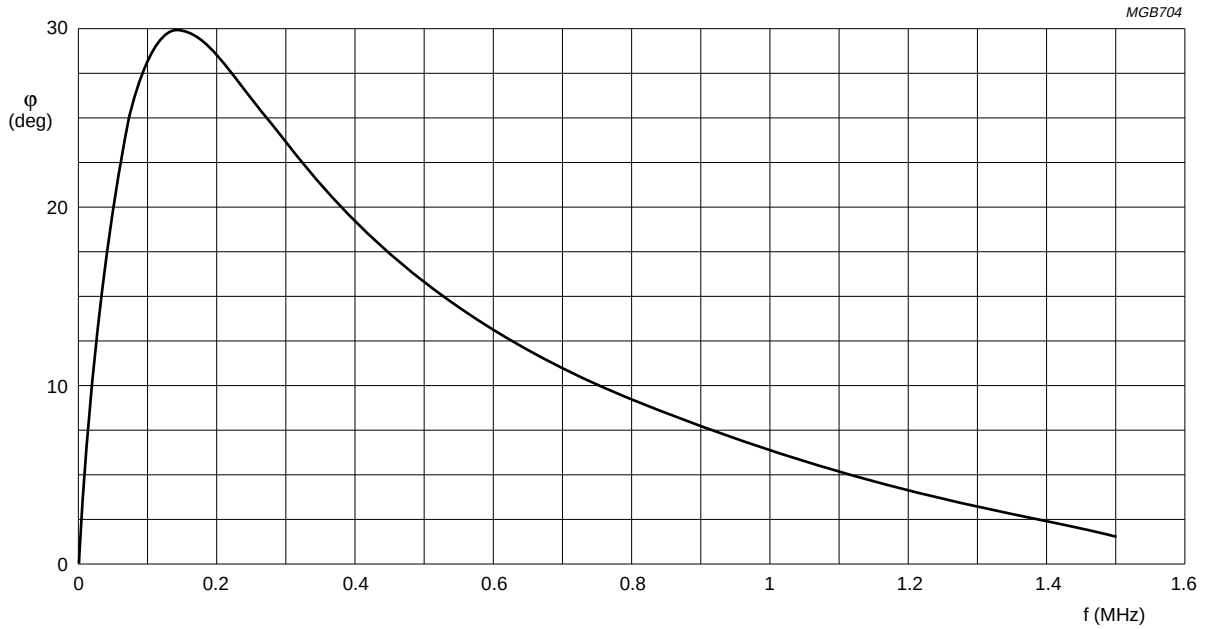


Fig.10 Phase of SECAM pre-emphasis.

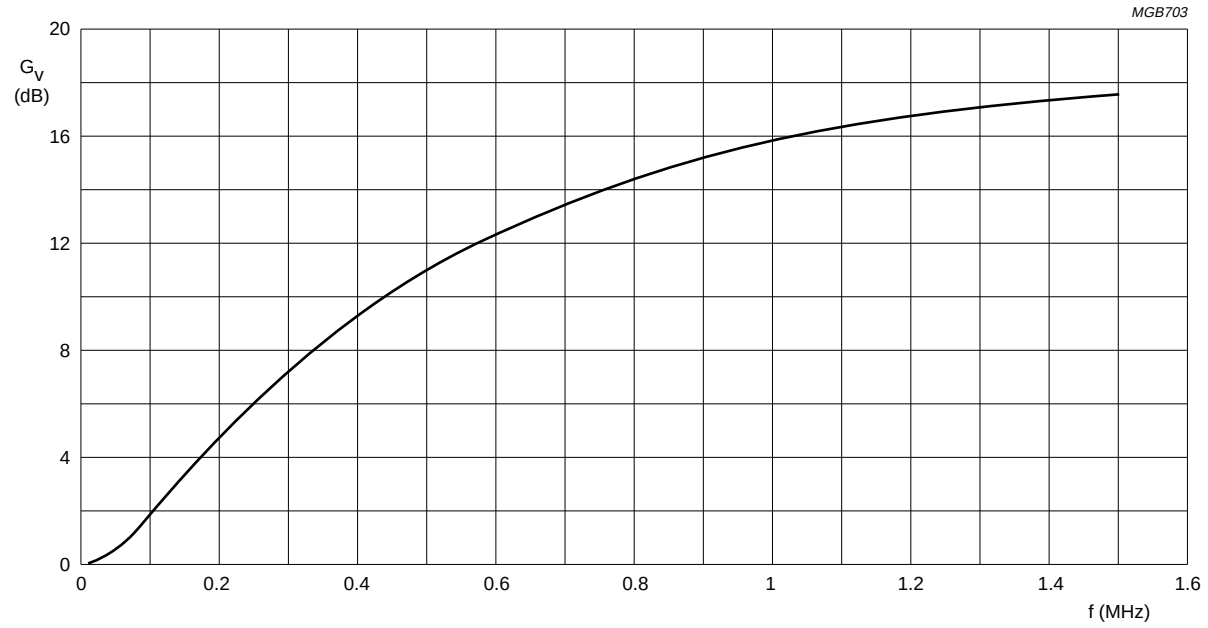


Fig.11 Gain of SECAM anti-Cloche.

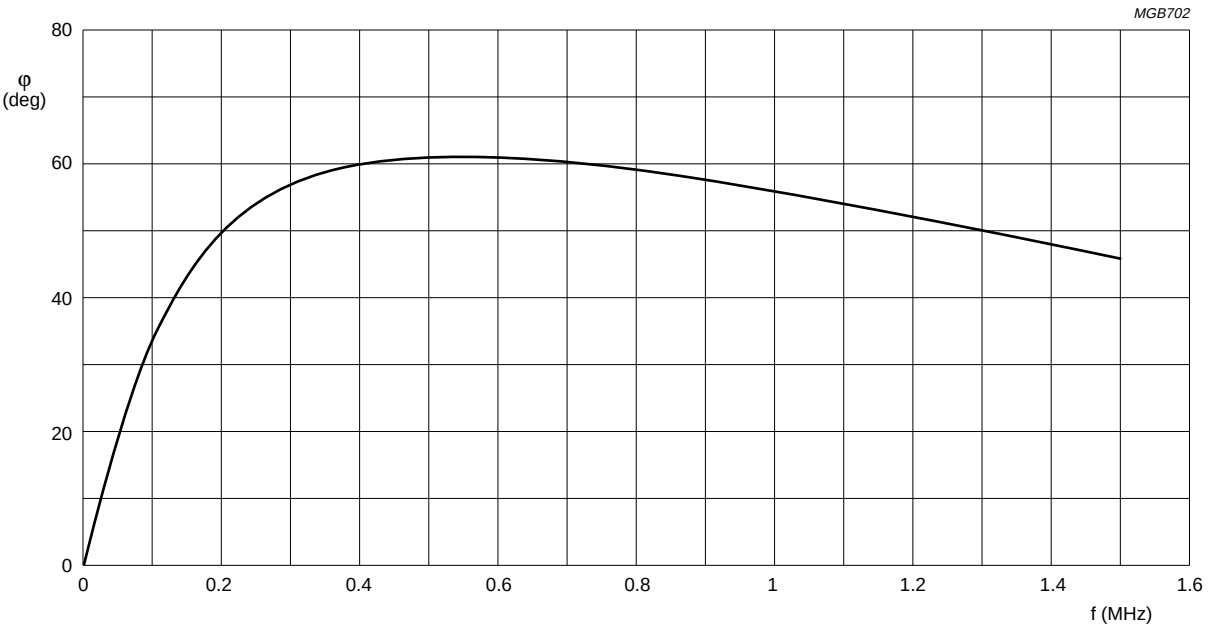


Fig.12 Phase of SECAM anti-Cloche.

CHARACTERISTICS

V_{DDD} = 4.75 to 5.25 V; T_{amb} = 0 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply					
V_{DDD}	digital supply voltage		4.75	5.25	V
V_{DDA}	analog supply voltage		4.75	5.25	V
I_{DDD}	digital supply current	note 1	–	250	mA
I_{DDA}	analog supply current	note 1	–	110	mA
Inputs					
V_{IL}	LOW level input voltage (except SDA, SCL, AP, SP and XTALI)		–0.5	+0.8	V
V_{IH}	HIGH level input voltage (except LLC, SDA, SCL, AP, SP and XTALI)		2.0	V_{DDD} + 0.5	V
	HIGH level input voltage (LLC)		2.4	V_{DDD} + 0.5	V
I_{LI}	input leakage current		–	1	µA
C_I	input capacitance	clocks	–	10	pF
		data	–	8	pF
		I/Os at high impedance	–	8	pF
Outputs					
V_{OL}	LOW level output voltage (except SDA and XTALO)	note 2	0	0.6	V
V_{OH}	HIGH level output voltage (except LLC, SDA, and XTALO)	note 2	2.4	V_{DDD} + 0.5	V
	HIGH level output voltage (LLC)	note 2	2.6	V_{DDD} + 0.5	V
I^2C-bus; SDA and SCL					
V_{IL}	LOW level input voltage		–0.5	+1.5	V
V_{IH}	HIGH level input voltage		3.0	V_{DDD} + 0.5	V
I_I	input current	V_I = LOW or HIGH	–10	+10	µA
V_{OL}	LOW level output voltage (SDA)	I_{OL} = 3 mA	–	0.4	V
I_O	output current	during acknowledge	3	–	mA
Clock timing (LLC)					
T_{LLC}	cycle time	note 3	34	41	ns
δ	duty factor t_{HIGH}/T_{LLC}	note 4	40	60	%
t_r	rise time	note 3	–	5	ns
t_f	fall time	note 3	–	6	ns
Input timing					
t_{SU}	input data set-up time (any other except CDIR, SCL, SDA, $\overline{\text{RESET}}$, AP and SP)		6	–	ns
t_{HD}	input data hold time (any other except CDIR, SCL, SDA, $\overline{\text{RESET}}$, AP and SP)		3	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Crystal oscillator					
f_n	nominal frequency (usually 27 MHz)	3rd harmonic	–	30	MHz
$\Delta f/f_n$	permissible deviation of nominal frequency	note 5	–50	+50	10^{-6}
CRYSTAL SPECIFICATION					
T_{amb}	operating ambient temperature		0	70	°C
C_L	load capacitance		8	–	pF
R_S	series resistance		–	80	Ω
C_1	motional capacitance (typical)		1.5 –20%	1.5 +20%	fF
C_0	parallel capacitance (typical)		3.5 –20%	3.5 +20%	pF
Data and reference signal output timing					
C_L	output load capacitance		7.5	40	pF
t_{OH}	output hold time		4	–	ns
t_{OD}	output delay time		–	25	ns
CHROMA, Y, CVBS and RGB outputs					
$V_{o(p-p)}$	output signal voltage (peak-to-peak value)	note 6	1.9	2.1	V
R_I	internal serial resistance		18	35	Ω
R_L	output load resistance		80	–	Ω
B	output signal bandwidth of DACs	–3 dB	10	–	MHz
ILE	LF integral linearity error of DACs		–	±2	LSB
DLE	LF differential linearity error of DACs		–	±1	LSB

Notes

1. At maximum supply voltage with highly active input signals.
2. The levels have to be measured with load circuits of 1.2 kΩ to 3.0 V (standard TTL load) and C_L = 25 pF.
3. The data is for both input and output direction.
4. With LLC in input mode. In output mode, with a crystal connected to XTALO/XTALI duty factor is typically 50%.
5. If an internal oscillator is used, crystal deviation of nominal frequency is directly proportional to the deviation of subcarrier frequency and line/field frequency.
6. For full digital range, without load, V_{DDA} = 5.0 V. The typical voltage swing is 2.0 V, the typical minimum output voltage (digital zero at DAC) is 0.2 V.

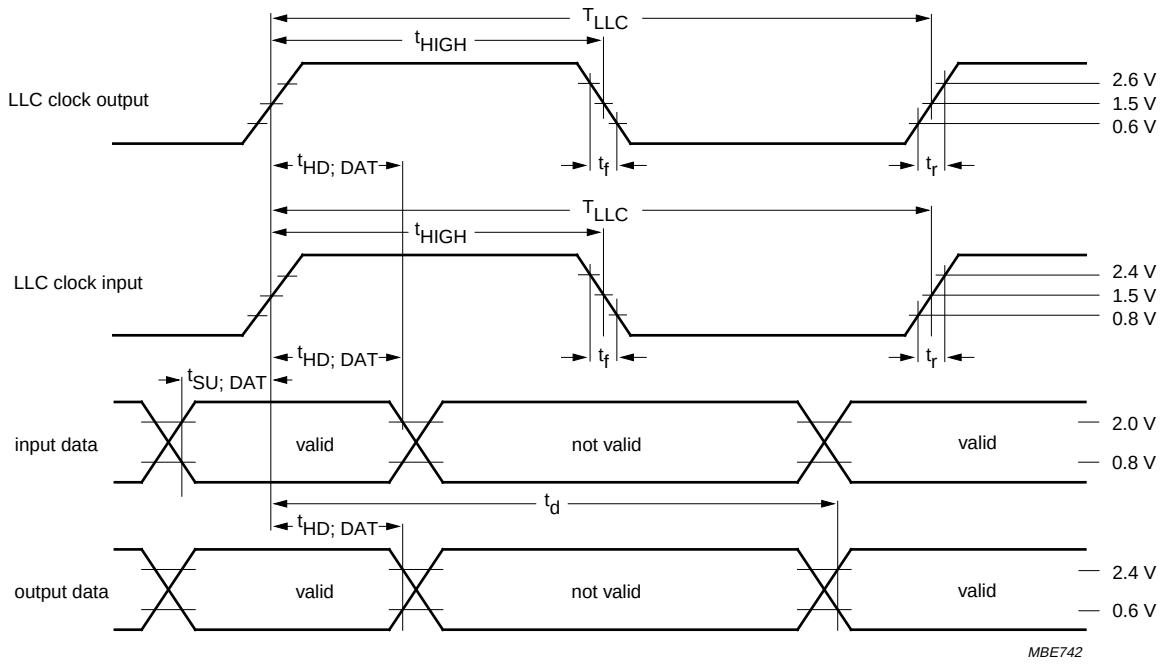
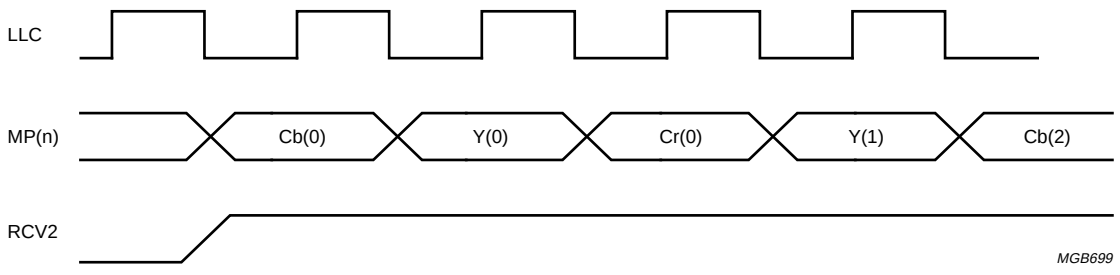
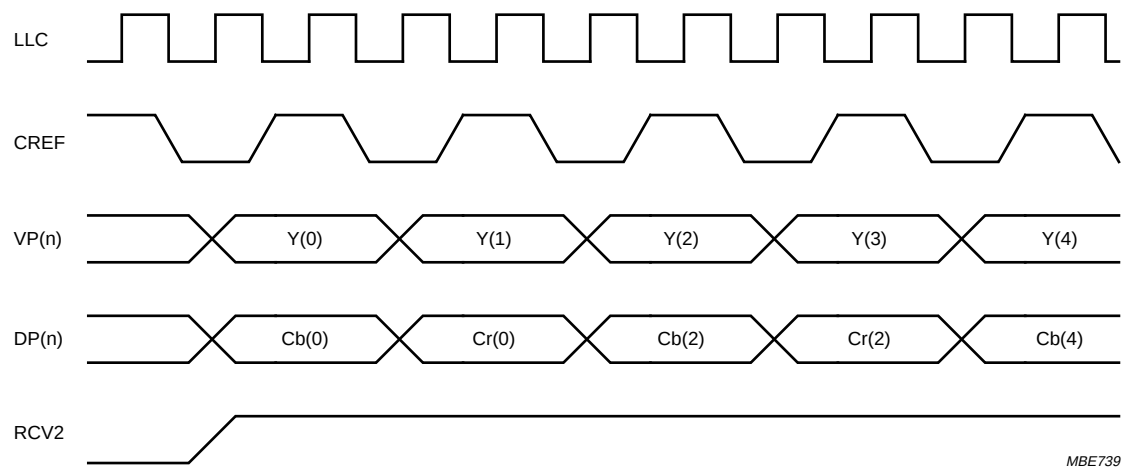


Fig.13 Clock data timing.



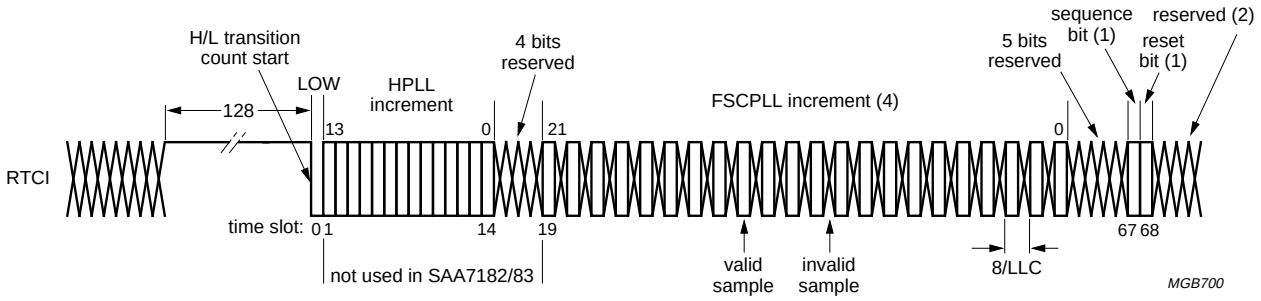
The data demultiplexing phase is coupled to the internal horizontal phase.
The phase of the RCV2 signal is programmed to 0F8h (110h for 50 Hz) in this example in output mode (RCV2S).

Fig.14 Functional timing.



The data demultiplexing phase is coupled to the internal horizontal phase.
The C_{ref} signal applies only for the 16 line digital TV format, because these signals are only valid in 13.5 MHz.
The phase of the RCV2 signal is programmed to 0F2h (110h for 50 Hz) in this example in output mode (RCV2S).

Fig.15 Digital TV timing.



(1) Sequence bit:
PAL = logic 0 then (R – Y) line normal; PAL = logic 1 then (R – Y) line inverted.
NTSC = logic 0 then no change.
(2) Reserved bits: 235 with 50 Hz systems; 232 with 60 Hz systems.
(3) Only from SAA7111 decoder.
(4) SAA7111 provides (22 : 0) bits, resulting in 3 reserved bits before sequence bit.

Fig.16 RTCI timing.

Teletext timing

Time t_{FD} is the time needed to interpolate input data TTX and inserting it into the CVBS and Y output signal, such that it appears at t_{TTX} = 10.2 µs after the leading edge of the horizontal synchronization pulse.

Time t_{PD} is the pipeline delay time introduced by the source that is gated by TTXRQ in order to deliver TTX data.

Since the pulse representing the TTXRQ signal is fully programmable in duration and rising/falling edges (TTXHS and TTXHE), it always can be ensured that the TTX data is inserted at the correct position of 10.2 µs after the leading edge of outgoing horizontal synchronization pulse.

Time t_{TTXWin} is the internally used insertion window for TTX data; it has a constant length that allows insertion of 360 teletext bits (maximum) at a text data rate of 6.9375 bits/s. The insertion window is not opened if the control bit TTXEN is zero.

TELETEXT PROTOCOL

The frequency relationship between TTX bit clock and the system clock LLC for 50 Hz field rate is given by the relationship of line frequency multiples, which means 1728/444.

Thus 37 TTX bits correspond to 144 LLC clocks, each bit has a duration of nearly 4 LLC clocks. The chip-internal sequencer and variable phase interpolation filter minimizes the phase jitter, and thus generates a bandwidth limited signal, which is digital-to-analog converted for the CVBS and Y outputs.

At the TTX input, bit duration scheme repeats after 37 TTX bits or 144 LLC clocks. The protocol demands that TXX bits 10, 19, 28 and 37 are carried by three LLC samples, all others by four LLC samples. After a cycle of 37 TTX bits, the next bits with three LLC samples are bits 47, 56, 65 and 74; this scheme holds for all succeeding cycles of 37 TTX bits, until 360 TTX bits (including 16 run-in bits) are completed. For every additional line with TTX data, the bit duration scheme starts in the same way.

Using appropriate programming, all suitable lines of the odd field (TTXOVS and TTXOVE) plus all suitable lines of the even field (TTXEVS and TTXEVE) can be used for teletext insertion.

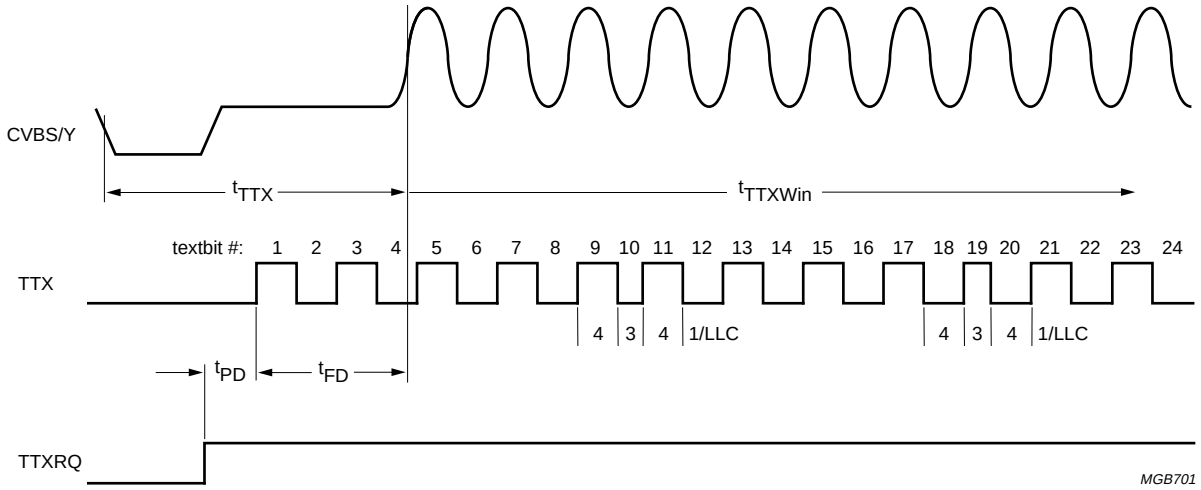


Fig.17 Teletext timing diagram.

APPLICATION INFORMATION

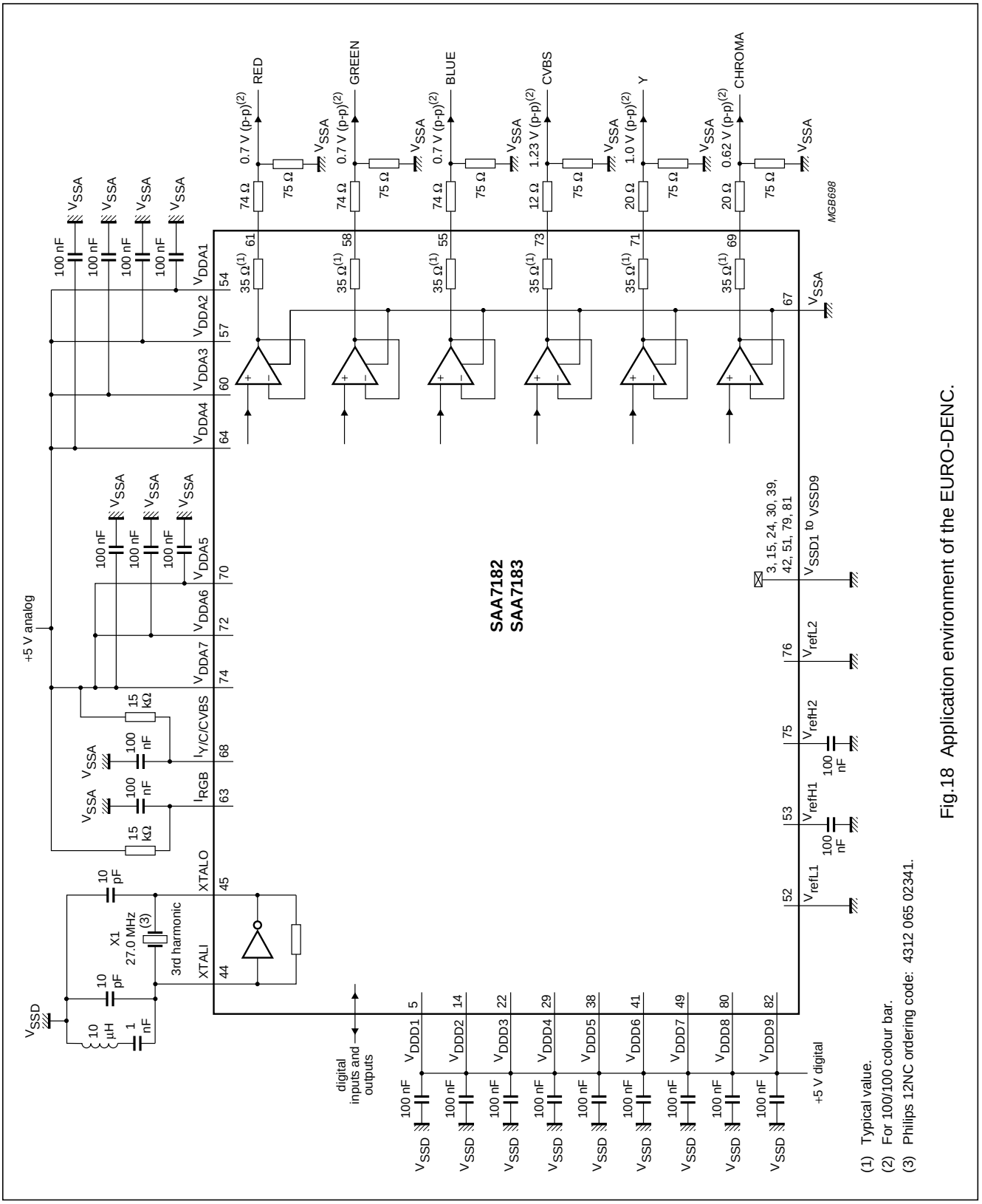
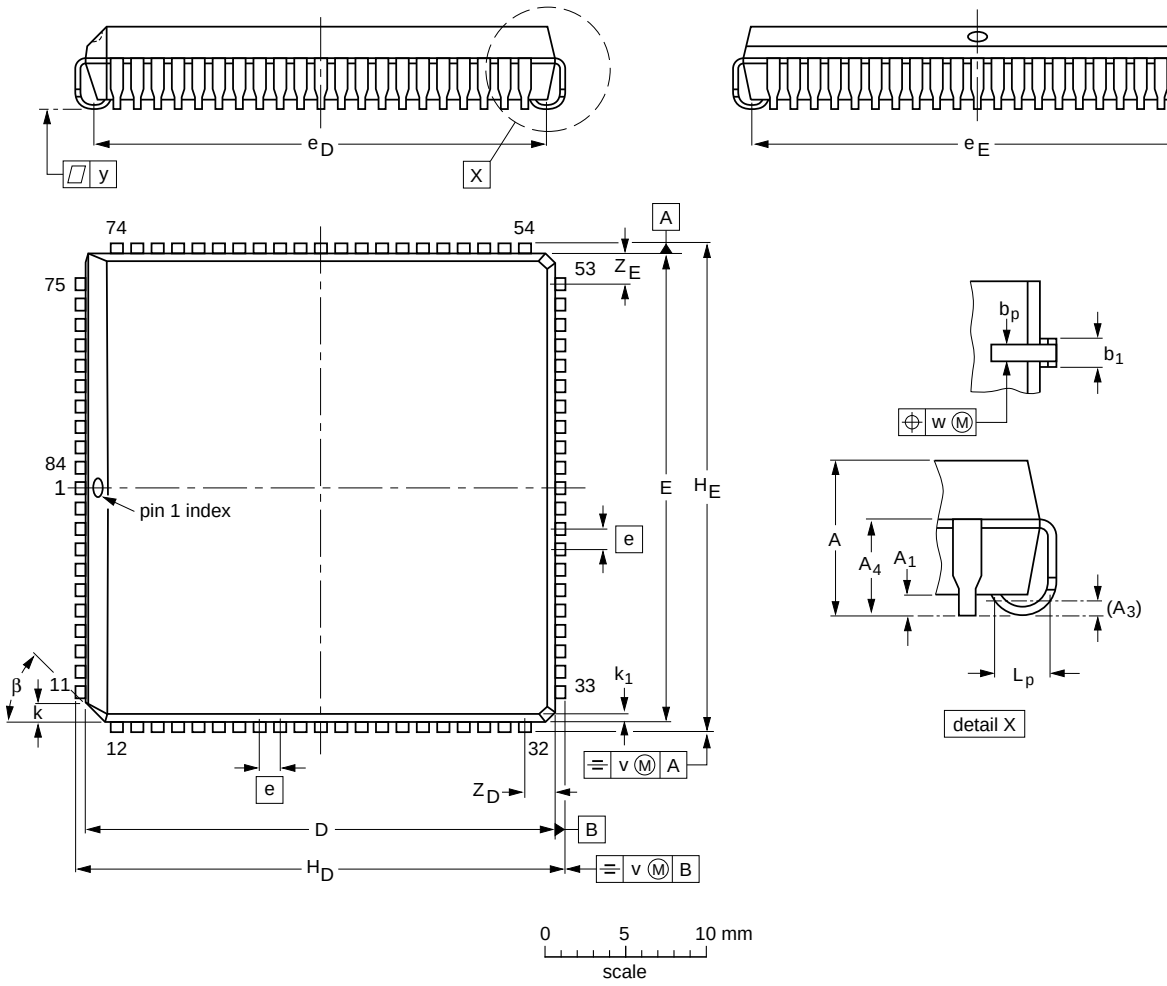


Fig.18 Application environment of the EURO-DENC.

(1) Typical value.
(2) For 100/100 colour bar.
(3) Philips 12NC ordering code: 4312 065 02341.

PACKAGE OUTLINE

PLCC84: plastic leaded chip carrier; 84 leads **SOT189-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.30	0.53 0.33	0.81 0.66	29.41 29.21	29.41 29.21	1.27	28.70 27.69	28.70 27.69	30.35 30.10	30.35 30.10	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45^o
inches	0.180 0.165	0.020	0.01	0.13	0.021 0.013	0.032 0.026	1.158 1.150	1.158 1.150	0.05	1.130 1.090	1.130 1.090	1.195 1.185	1.195 1.185	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT189-2						~~92-11-17~~ 95-03-11

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

NOTES

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